REMARKS

Applicant has carefully reviewed this Application in light of the Final Office Action mailed April 8, 2005. Claims 1 and 3-5 are pending in this Application. Claims 2 and 6-7 were previously cancelled without prejudice or disclaimer. Claims 1 and 3-5 stand rejected under 35 U.S.C. §102(b). Applicant respectfully requests reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 102

Claims 1 and 3-5 were rejected by the Examiner under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,945,507 issued to Ryuji Ishida et al. ("*Ishida*").

Ishida discloses an overflow correction circuit for use in an arithmetic operation circuit. Specifically, *Ishida* discloses an adder 10 whose output 22 can be detected for an overflow condition by detector 34. Depending upon the type of overflow condition, overflow detector 34 then directs the selector to forward one of three values (the maximum value 28, the minimum value 32 or the results of the adder 10) to the accumulator 46.

Claim 1 recites a system comprising "logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison."

Applicant respectfully submits that the cited reference fails to disclose each and every element of Applicant's invention. *Ishida* fails to teach a system for overflow and saturation processing comprising "logic means for comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison," as recited by amended Claim 1. In the Final Office Action, the Examiner states that *Ishida* teaches "logic means (Figure 2 particularly 66) for comparing most significant bits of the guard bits and most significant bit [sic] of the result of the added operands and for generating the control signals (40 and 42) in accordance with the comparison." (Final Office Action, Page 3). *Ishida*, however, does not disclose comparing most significant bits of the guard bits and most significant bits of the result of the added operands. The Examiner stated that the guard bits, as disclosed by *Ishida*, are D22 and D23 as illustrated in Figure 2. (Final Office Action, Page 2). *Ishida*, however, describes D22 and

D23 as the high place two bits of the output of adder 10. (Col. 4, Lines 41-43). Figure 2 illustrates a comparison of the high place two bits D22 and D23 with a correction mode signal. *Ishida*, therefore, fails to teach or suggest "comparing most significant bits of the guard bits and most significant bits of the result of the added operands, and for generating the control signals in accordance with the comparison," as recited in Claim 1. The cited reference fails to disclose the recited limitations and, therefore, cannot anticipate Claim 1.

Given that Claims 3-5 depend from Claim 1, Applicant respectfully submits that Claims 3-5 are allowable. As such, Applicant respectfully requests that the Examiner withdraw the rejections and allow Claims 1 and 3-5.

Information Disclosure Statement

Applicant would like to bring to the Examiner's attention that the Examiner made no indication that References "A-I" on Page 4 submitted with Information Disclosure Statement and PTO Form 1449 filed on February 15, 2005, had been considered in the Final Office Action mailed April 8, 2005. Applicant respectfully requests confirmation of the consideration of References "A-I" on Page 4. Applicant attaches a copy of the PTO Form 1449 that was attached to the Final Office Action mailed April 8, 2005, and respectfully requests that the Examiner place his initials next to References "A-I" if citation is to be considered or draw a line through the citation if the citation is not to be considered.

CONCLUSION

Applicant appreciates the Examiner's careful review of the application. Applicant has now made an earnest effort to place this case in condition for allowance in light of the amendments and remarks set forth above. For the foregoing reasons, Applicant respectfully requests reconsideration of the rejections and full allowance of Claims 1 and 3-5.

Applicant believes there are no fees due at this time, however, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-2148 of Baker Botts L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicant's attorney at 512.322.2581.

Respectfully submitted,
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Date: June 8, 2005

PTO-1449

Information Disclosure Citation in an Application

Application No.	Applicant(s)		
09/870,944	Michael I. Catherwood		
Docket Number	**Group Art Unit**	**Filing Date**	
068354.1443	2124	June 1, 2001	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A.	6356970	3/12/02	Killian et al.	~~710~~	~~269~~	5/28/99
	B.	6397318	5/28/02	Peh	~~711~~	~~220~~	4/2/98
	C.	2002/0194466	12/19/02	Catherwood et al.	~~712~~	~~241~~	6/1/01
	D.	2003/0093656	5/15/03	Masse et al.	~~712~~	~~241~~	10/1/99
	E.	6658578	12/2/03	Laurenti et al.	~~713~~	~~324~~	10/1/99
	F.	6681280	1/20/04	Miyake et al.	~~710~~	~~261~~	10/4/00
	G.	6728856	4/27/04	Grosbach et al.	~~711~~	~~202~~	6/1/01
	H.	6763478	7/13/04	Vinh X. Bui	~~713~~	~~600~~	10/24/00
	I.	6751742	6/15/04	Duhault et al.	~~713~~	~~323~~	8/31/99
	J.						
	K.						
	L.						
	M.						
	N.						
	O.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	P.							
	Q.							
	R.							

NON-PATENT DOCUMENTS - DOCUMENT (Including Author, Title, Source, and Pertinent Pages)

	S.	
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	W.	
	X.	
	Y.	
	Z.	

EXAMINER	DATE CONSIDERED
	03/10/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.